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## **About us**

Infinior MicroSystems was founded in April 2000 to provide competitive and high-performance core solution. Infinior microsystems is a fast growing, technology company dedicated to provide a complete and cost-effective general purpose embedded microprocessor and DSP solutions for explosive growth of embedded systems in high volume market.

Infinior MicroSystems expects to establish itself as a leading player in MCU market and to be the leader in providing highly integrated cutting edge core silicons and IPs using proprietary technologies and core advanced design methodologies.

Infinior MicroSystems designs, develops and supplies complete embedded networking system silicon solutions including CISC, RISC and DSP, and related applications including operating systems and stacks.

## **Business Scope**

- Offers cutting edge processor core based high performance standard silicon products
- offers leading edge and valuable proven processor core IPs
- offers embedded system solution for emerging application

## **History**

- ▶ APR. 2000 Founded Infinior MicroSystems Co., Ltd.
- ▶ JUN. 2000 Designated as Technical Finance-supporting company by Korea Industry Bank & Korea Credit Guarantee Fund
- ▶ JUL. 2000 Established R&D Center (Registered Industry & Technology Promotion Association)
- ▶ DEC. 2000 Appointed Military Exception Enterprise by the Office of Military Manpower
- ▶ MAR. 2001 Designated as a Venture Company by Technology Appraisal of KOTEC (Korea Technology Credit)
- ▶ APR. 2001 Announced IMS16B<sup>\*</sup>-Tahoe 16bit Embedded Microprocessor
- ▶ MAY. 2001 Designated as Science Technical Promotion Finance-supporting company by Technology Appraisal Guarantee of KOTEC
- ▶ MAY. 2001 Designated as a Superior Technology Companies by KOTEC
- ▶ DEC. 2001 Raised seed round investment led by Hanmi Technology Investment Co., Ltd. Hanhwa VC Corp. and Venture Line Inc.
- ▶ DEC. 2001 Distribution Channel Agreement with T&C Semitech in Korea
- ▶ JAN. 2002 Announced IMS5016E<sup>\*</sup>-Meridian Multimedia Processor
- ▶ JUN. 2002 Announced IMS16C<sup>\*</sup>-Tornado Enhanced 16bit Embedded Microprocessor
- ▶ OCT. 2002 Distribution Channel Agreement with VAS Corporation in Korea
- ▶ OCT. 2002 Awarded Digital Innovation Prize sponsored by Korean daily news paper

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# IMS16B-Tahoe Microcontroller



## FEATURE

### Compatibility

- 100% software compatible with x86(i8086/i80186) real mode
- Supported by widely available native x86 development tools (e.g. MASM, TASM, ...)

### Technology

- Fully synchronous and static design
- 60MHz operation in 3.3 Volt
- 0.5um 3.3V static CMOS process
- 128-pin QFP (1420 type, Quad Flat Package)

### Core

- 1Mega Byte memory address space
- 64K byte I/O space
- 16-bit Multiplexed AD(Address & Data) Bus
- Non-Multiplexed 20 Bit Address Bus
- Glueless Bus interface to external memory systems

### Peripheral

#### Chip select

- 1 Upper Memory Chip Select (Ending address is fixed at FFFFh)
- 1 Lower Memory Chip Select (Starting address is fixed at 00000h)
- 6 Peripheral Chip Selects (Block size is fixed at 256 bytes)
- 4 Midrange Chip Selects (Starting address and block size are programmable)
- PCS and MCS Auxiliary (Affects both PCS and MCS)

#### Interrupt Control Unit

- 6 External Interrupts
  - 5 Maskable Interrupts
  - 1 Non-Maskable Interrupts
- 6 Internal Interrupts
  - 3 Timers
  - 2 DMA Channels
  - 1 UART Serial port
- Supports Master Mode and Fully Nested Mode
- Programmable Interrupt Priority

#### Timer Control Unit

- 16 Bit Programmable 3 Timers
  - 2 External Timers
  - 1 Internal Watch Dog Timer



#### Serial Port Interface

- 1 Async. Serial port
  - Full duplex operation
  - 7, 8-bit data transfer
  - Odd parity, Even parity or No parity
  - 1 or 2 stop bits
  - Loop back mode
  - Ability to break character transmit
  - Does not contain DMA support
- 1 Sync. Serial port
  - Operates as the master port

#### 32 User Programmable I/Os

#### SDRAM Control Unit

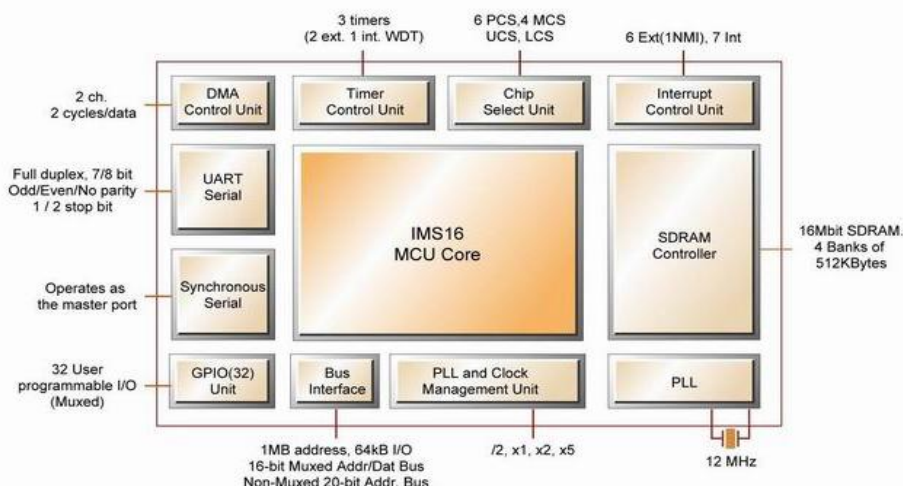
- Support 1Mb x 16 SDRAM
- Support 4 Banks (512KB x 4 Bank)

#### PLL Management Unit

- 1/2, x2, x5

#### DMA Control Unit

- Provides 2 high-speed DMA channels
- Data transfer can occur between memory and I/O space
- Two Bus cycles are necessary for each data transfer



Block Diagram of IMS16B

### Software Development Environment

- Startup code\_ Boot loader
- RTOS (Any x86 16bit core supporting OS)
- Cross Compiler (dev86, Borland C/C++, Visual C/C++, Locator, Paradigm..)
- Stacks (LAN driver(RTL8019, CS8900), IP/TCP, UDP/FTP, Web Server, DHCP, ATA-4/FAT32 file system)



# IMS16C-Tornado Microcontroller

## FEATURE

### Compatibility

- 100% software compatible with x86/x88 (i80186/i80188) real mode
- Supported by widely available native x86 development tools (e.g. MASM, TASM, ...)

### Technology

- Fully synchronous and static design
- 90MHz operation in 3.3 Volt
- 0.35um 3.3V static CMOS process
- 3.3V I/O Pad (5V tolerant I/O)
- 128-pin QFP (Quad Flat Package)

### Core

- 90MHz operation with 3 cycle access (T1, T2, T3)
- Byte/Word operation. (80186 mode, 80188 mode)
- 1M Byte memory address space, 64K byte I/O space
- Non-multiplexed 20-bit Address Bus
- SDRAM address shares with Address bus
- Internal 16KB RAM in LCS Area

## Peripheral

### Chip select

- 1 Upper Memory Chip Select (Ending address is fixed at FFFFh)
- 1 Lower Memory Chip Select (Starting address is fixed at 00000h)
- 6 Peripheral Chip Selects (Block size is fixed at 256 bytes)
- 4 Midrange Chip Selects (Starting address and block size are programmable)
- PCS and MCS Auxiliary (Affects both PCS and MCS)

### Interrupt Control Unit

- 6 External Interrupts
  - 5 Maskable Interrupts
  - 1 Non-Maskable Interrupts
- 10 Internal Interrupts
  - 3 Timers
  - 2 DMA Channels
  - 3 UART Serial ports
  - 2 HDLC controllers
- Supports Master Mode and Fully Nested Mode
- Programmable Interrupt Priority

### Timer Control Unit

- Three 16 Bit Programmable Timers
  - 2 External Timers
  - 1 Internal Watch Dog Timer

### Two internal Single Port Sync RAM

- 16 Kbytes On-Chip RAM in LCS area

### DMA Control Unit

- Shares Two high-speed DMA channels with UART serial port
- Data transfer can occur between memory and I/O space
- Two Bus cycles are necessary for each data transfer

### PLL Management Unit

- 1/2, MD1 (81.1MHz), MD2 (90.3MHz) and x6

## Software Development Environment

- Startup code\_ Boot loader
- RTOS (Any x86 16bit core supporting OS)
- Cross Compiler (dev86, Borland C/C++, Visual C/C++, Locator, Paradigm..)
- Stacks (LAN driver(RTL8019, CS8900), IP/TCP, UDP/tFtp, Web Server, DHCP, ATA-4/FAT32 file system)

### 3 UART Serial Port Interface

- Full duplex operation
- 7, 8-bit data transfer
- Odd parity, Even parity or No parity
- 1 or 2 stop bits
- Loop back mode
- Ability to break character transmit
- 2 UART port with DMA operation
- 1 UART port with normal operation

### 44 User Programmable I/Os

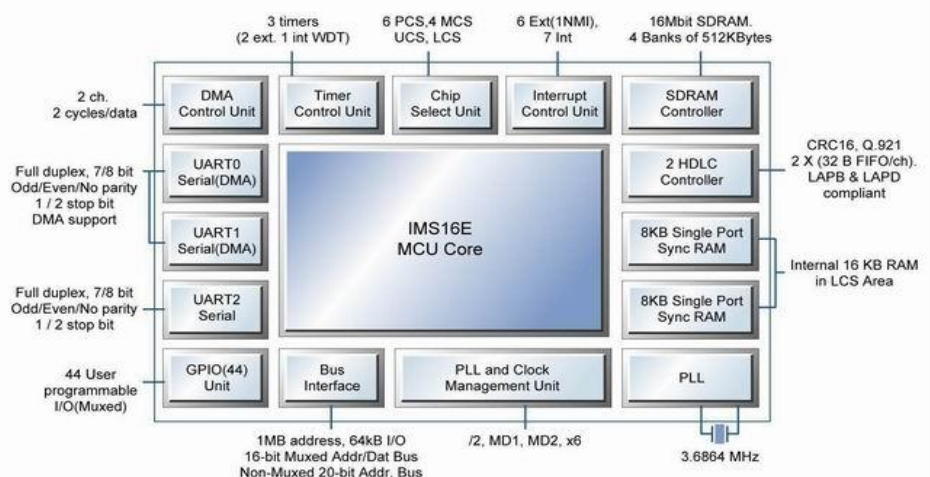
### SDRAM Control Unit

- Support 4 Banks (512Kbytes each) or
- Support 2 Banks (960Kbytes each)

### 2 HDLC Control Units

- CRC-CCITT, CRC16, Two 64 Bytes FIFO/ch. Q921. LAPB and LAPD compliant

### Sixteen 16-bit General Purpose Registers



Block Diagram of IMS16C

# IMS16N-Spider Microcontroller



## FEATURE

### Compatibility

- 100% software compatible with x86/x88 (i80186/i80188) real mode
- Supported by widely available native x86 development tools (e.g. MASM, TASM,...)

### Technology

- Fully synchronous and static design
- 100MHz operation in 3.3 Volt
- 0.35um 3.3V static CMOS process
- 3.3V I/O Pad (5V tolerant I/O)
- 144-pin QFP (Quad Flat Package)

### Peripheral

#### Chip select

- 1 Upper Memory Chip Select
- 1 Lower Memory Chip Select
- 6 Peripheral Chip Select
- 4 Midrange Chip Select

#### Interrupt Control Unit

- 6 External Interrupts
  - 5 Maskable Interrupts
  - 1 Non-Maskable Interrupts
- 11 Internal Interrupts
  - 3 Timers
  - 2 DMA Channels
  - 3 UART. Serial port
  - 1 MAC controller
  - 1 USB controller
- Supports Master Mode and Fully Nested Mode
- Programmable Interrupt Priority

#### Timer Control Unit

- Three 16 Bit Programmable Timers
  - 2 External Timers
  - 1 Internal Watch Dog Timer

#### MAC Control Unit

- Support IEEE802.3/802.3u(10/100Mbps)
- Internal FIFO and DMA operation
- MII/7 wire PHY interface

#### SDRAM Control Unit

Bank Selection (16MB, 64MB, 128MB)

### Core

- 100MHz operation with 3 cycle access (T1, T2, T3)
- Byte/Word operation. (80186 mode, 80188 mode)
- 16M Byte memory address space, 64K byte I/O space
- Non-multiplexed 24-bit Address Bus
- SDRAM address shares with Address bus
- Two way set-associative 8 KB instruction Cache

#### 3 UART Serial Port Interface

Full duplex operation  
7, 8-bit data transfer  
Odd parity, Even parity or No parity  
1 or 2 stop bits  
Loop back mode  
Ability to break character transmit

- 2 UART port with DMA operation
- 1 UART (16C550 Full Compliant) with FIFO

#### 1 Sync. Serial Port Interface

Operates as the master port

#### I<sup>2</sup>C Interface

#### 48 User Programmable I/Os

#### E-IDE Interface (Pin share with SDRAMC)

#### USB 1.1 with PHY

Bulk mode only (device)

#### Sixteen 16-bit General Purpose Registers

#### PLL Management Unit

- 1/2, MD1 (100MHz), x6, User Programmable

#### Watch Dog Timer

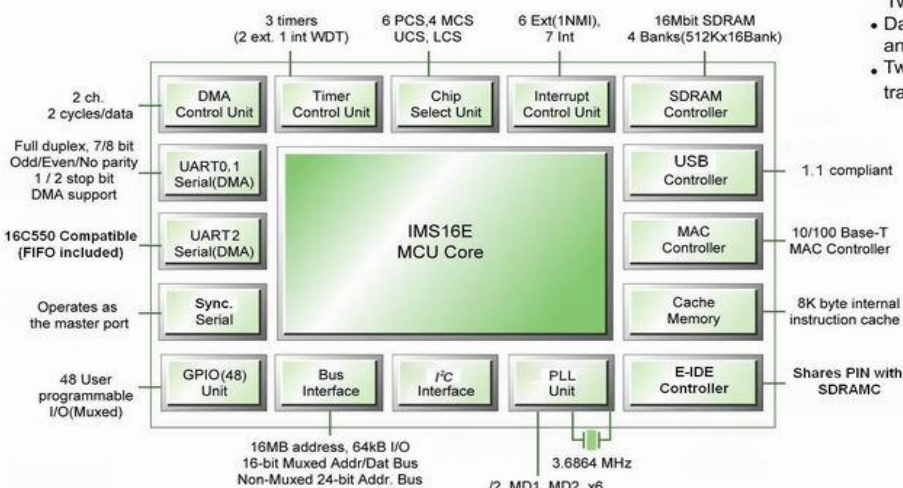
- WDT out pin support (connected to NMI when using WDT)
- External reset period selection

#### DMA Control Unit

- Shares two high-speed DMA channels with Two UART serial ports
- Data transfer can occur between memory and I/O space
- Two Bus cycles are necessary for each data transfer

### Software Development Environment

- Startup code\_ Boot loader
- RTOS (Any x86 16bit core supporting OS)
- Cross Compiler (dev86, Borland C/C++, Visual C/C++, Locator, Paradigm..)
- Stacks (LAN driver(RTL8019, CS8900), IP/TCP, UDP/tFtp, Web Server, DHCP, ATA-4/FAT32 file system)



Block Diagram of IMS16N

# IMS5016E-Meridian Multi core processor



## FEATURE

### Compatibility

- 100% software compatible with intel® x86 real mode instructions
- DSP co-processor supports variety of instructions suitable for highly complex arithmetic operations (100% compatible with TI c54X®)

### Operation Modes

IMS5016E has three-operation mode, i.e. MCU single mode, DSP single mode and dual mode.

Each mode can be configured through external or internal configurations.

When IMS5016E runs in dual mode, MCU and DSP work as loosely coupled multiprocessor and communicate with each other over shared memories.

### DSP Single mode

- 16 bit Fixed Point Digital Signal Processor
- 16.7 ns single cycle execution (60 MIPS Operation)
- 6 Stage Pipelines (Pre-fetch, Fetch, Decoder, Access, Read, Execute)
- Advanced Multi-bus Harvard architecture with Three 16 bit Data Buses and One Program Bus
- 64K words Program, Data, I/O Space.
- 4K words internal program ROM
- 10K word internal program/data Two-Port RAM
- 40bit Arithmetic Logic Unit including One Barrel Shifter and Two independent 40-bit Accumulators
- 17 x 17 Parallel Multiplier Coupled to a 40bit dedicated Adder
- Compare Select and Store Unit, Exponent Encoder in a Single Cycle
- Two Address Generators with Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units
- Instruction with 32bit Long Word Operand
- Arithmetic Instruction with Parallel Store and Parallel Load
- Buffered Serial Port
- Parallel Host Port Interface
- Interrupt Controller
- Timer

### Technology

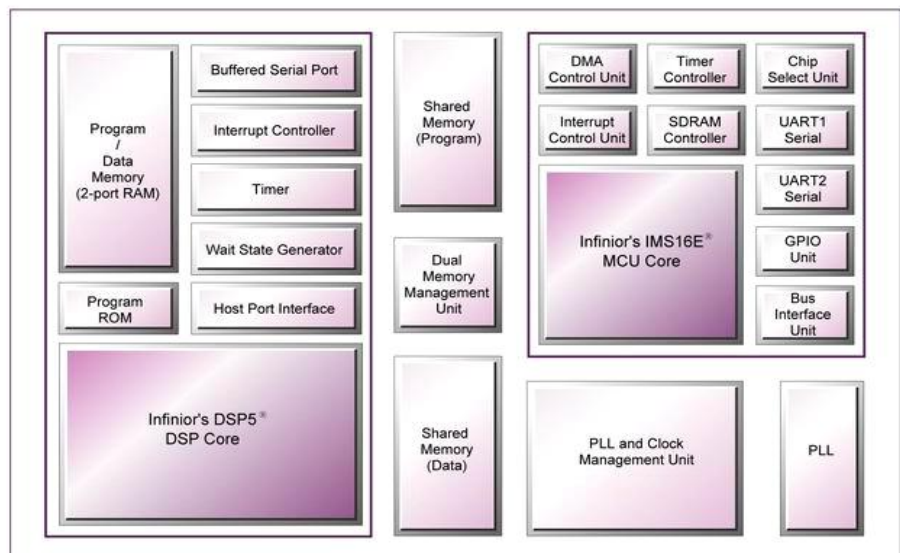
- Fully Synchronous and Static Design
- 0.35um, 3.3V static CMOS Technology
- 60Mhz operation at Dual mode (MCU+DSP)
- 80Mhz operation at MCU mode (MCU only)
- 60Mhz operation at DSP mode (DSP only)
- 3.3V I/O Pad (5V Tolerant)
- 240 Pin Plastic Quad Flat Package (PQFP)

### MCU Single mode

- 100% software compatible with the Intel i8086/i80186\* Supported by widely available native x86 development tools)
- 80Mhz operation with 3-cycle access. (T1, T2, T3)
- Byte / Word Operation. (i80186\* mode, i80188\* mode)
- 1Mbyte Memory address space, 64Kbyte I/O space
- 16 bit ALU
- Peripheral Interface Logic
- Chip-Select and Ready Control Logic
- 2 Channel DMA Controllers
- 3 Programmable 16-bit Timers
- Interrupt Controller
- Refresh Control Unit
- Power Save Logic
- Chip Select Unit
- 2 UART Serial Ports
- General Purpose Programmable I/O (GPIO)
- SDRAM Controller (16Mbits SDRAM Support with 4\*512kbytes with bank selection)

### MCU Single mode

- MCU can access internal DSP memory through Host Port Interface.
- MCU can read and write shared memory (On chip 32kbytes Synchronous RAM)
- MCU can control shared memory occupation with DMCR memory mapped register.
- MCU can control DSP with reset, interrupt and DSP mode change (microprocessor mode, microcomputer mode)
- DSP can read and write shared memory.



Block Diagram of IMS5016E



## DSP (Digital Signal Processor)

### DSP2

Infinior MicroSystems' DSP2<sup>®</sup> is a general-purpose compact sized 16-bit fixed point digital signal processor core.

It has been designed in synthesizable HDL and can be configured with variety of on-chip memories and peripherals.

Then it can be used as an ASIC library element in a variety of DSP applications.

This core approach gives both operational flexibility and numerical capability to the system designer.

### DSP5

Infinior MicroSystems' DSP5<sup>®</sup> is a high performance 16-bit fixed point digital signal processor core IP.

This is based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses.

This processor core provides an arithmetic logic unit (ALU) that has a high degree of parallelism, application-specific hardware logic, on-chip memory, and additional on-chip peripherals.

DSP5<sup>®</sup> also provides a highly specialized instruction set, which is the basis of the operational flexibility and speed of DSP.

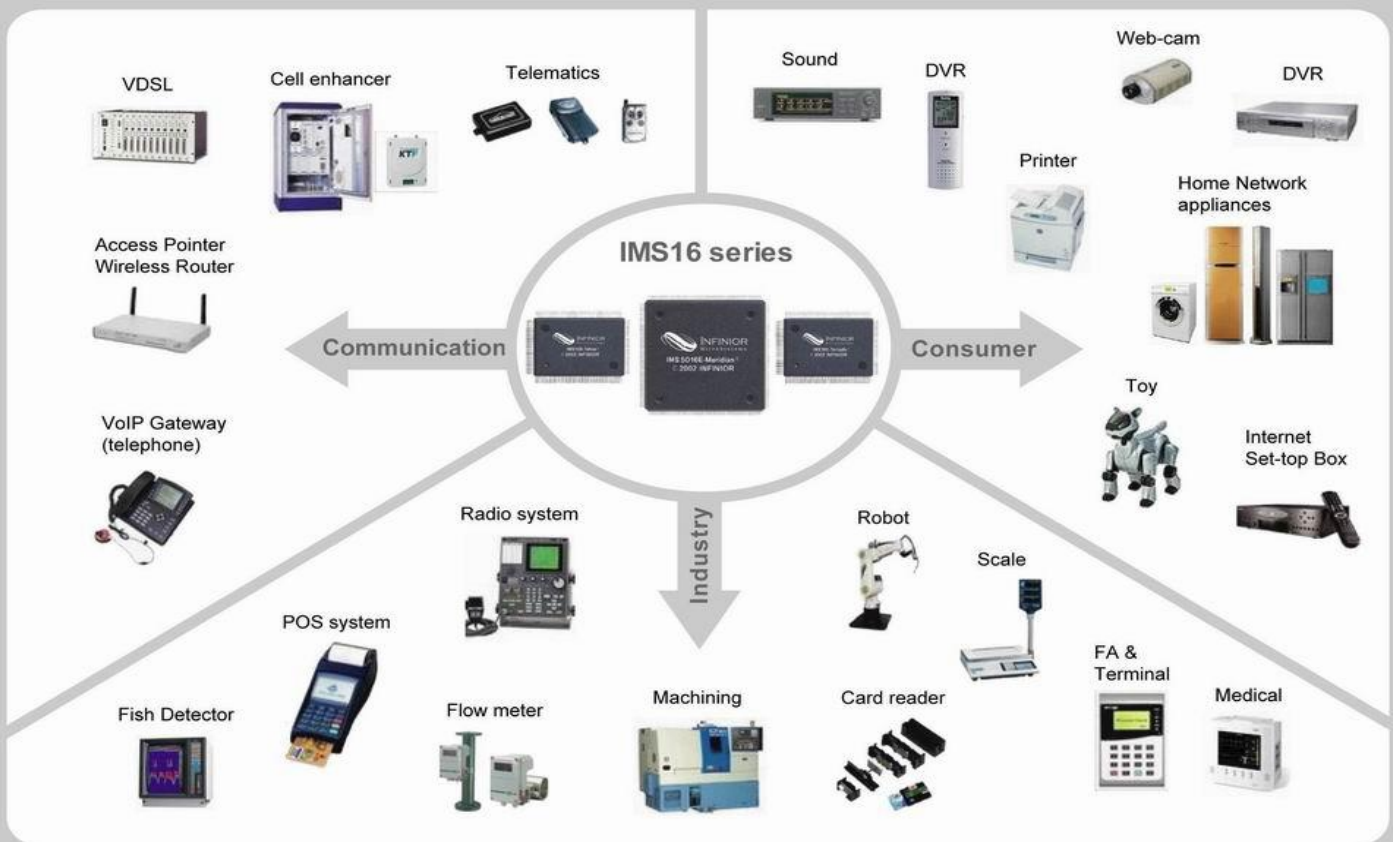
DSP5<sup>®</sup> is designed and prepared to be used as an ASIC library element in variety of DSP applications and SoC design.

This core approach gives both operational flexibility and numerical capability to the SoC designer.

The DSP5<sup>®</sup> core is proven at 0.35um static CMOS integrated-circuit technology.

It is designed to execute more than 70 MIPS.

## IMS16 series applications



## IMS16 Series Features



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FAX : 02-704-7211  
E-mail : jkang@vas.co.kr

	IMS16B	IMS16C	IMS16N
Speed	40/50/60MHz @3.3V	80/90MHz @3.3V	90/100MHz @3.3V
Address Bus	20bit	20bit	24bit
Data Bus	16bit	16bit	16bit
186/188 mode	186 mode only	186/188 mode	186/188 mode
Bus Timing	T1, T2, T3, T4	T1, T2, T3	T1, T2, T3
Wait State (UCS, LCS, MCS, PCS)	3, 3, 3, 7	15, 15, 15, 31	15, 15, 15, 31
5V Tolerant I/O	No	Yes	Yes
Package	128pin QFP 1420	128pin QFP 1420	144pin QFP
Power Consumption	1.65mA/Mhz at 3.3V	1.3mA/Mhz at 3.3V	
Deliverable	Silicon/IP/Verilog	Silicon/IP/Verilog	IP/Verilog
Available	Now	Now	4Q 2003

### Additional Peripherals

	IMS16B	IMS16C	IMS16N
UART	1	3	3
DMA Controller	2 External DMA	2 External DMA (2 UART DMA)	2 External DMA (2 UART DMA)
SDRAM Controller	Yes	Yes	Yes
GPIO	32	44	48
Internal GPR	No	16bit x 16 GPR	16bit x 16 GPR
Internal Memory	No	16K bytes Sync RAM	8K bytes Code Cache
Watch Dog Timer		Hardware	Hardware
Interrupt	6 Ext. / 1 NMI	6 Ext. / 1 NMI	6 Ext. / 1 NMI
HDLC Controller	No	2 channel with 4 x 32bytes FIFO	No
MAC Controller	No	No	10/100 BaseT, MII I/F
Address Range	1MB	1MB	16MB