DSP2®

Compact 16Bit Fixed Point DSP Core

General Description

Infinior MicroSystems' DSP2® is a general-purpose compact 16-bit fixed-point digital signal processor core. It has been designed in synthesizable HDL (Hardware Description Language) and can be configured with variety of on-chip memories and peripherals.

DSP2 adopts modified Harvard architecture, which enables high performance and provides cost effective design solution. Its compact instruction set also gives more flexibility to the software engineers.

DSP2 has capability of executing more than 100MIPS (Million Instructions Per Second) under 0.35um CMOS Process. Core gate counts is as small as 35K, which is not included memory modules. DSP2 is fully synchronous and static design with single internal clock and operates in 4 stages pipelines (Instruction Fetch, Decode, Operand Fetch, Executions).

DSP2 is targeted for small and high performance digital signal processing ASSP (Application Specific Standard Product) and can be used as an ASIC library element in a variety of DSP (Digital Signal Processor) applications.

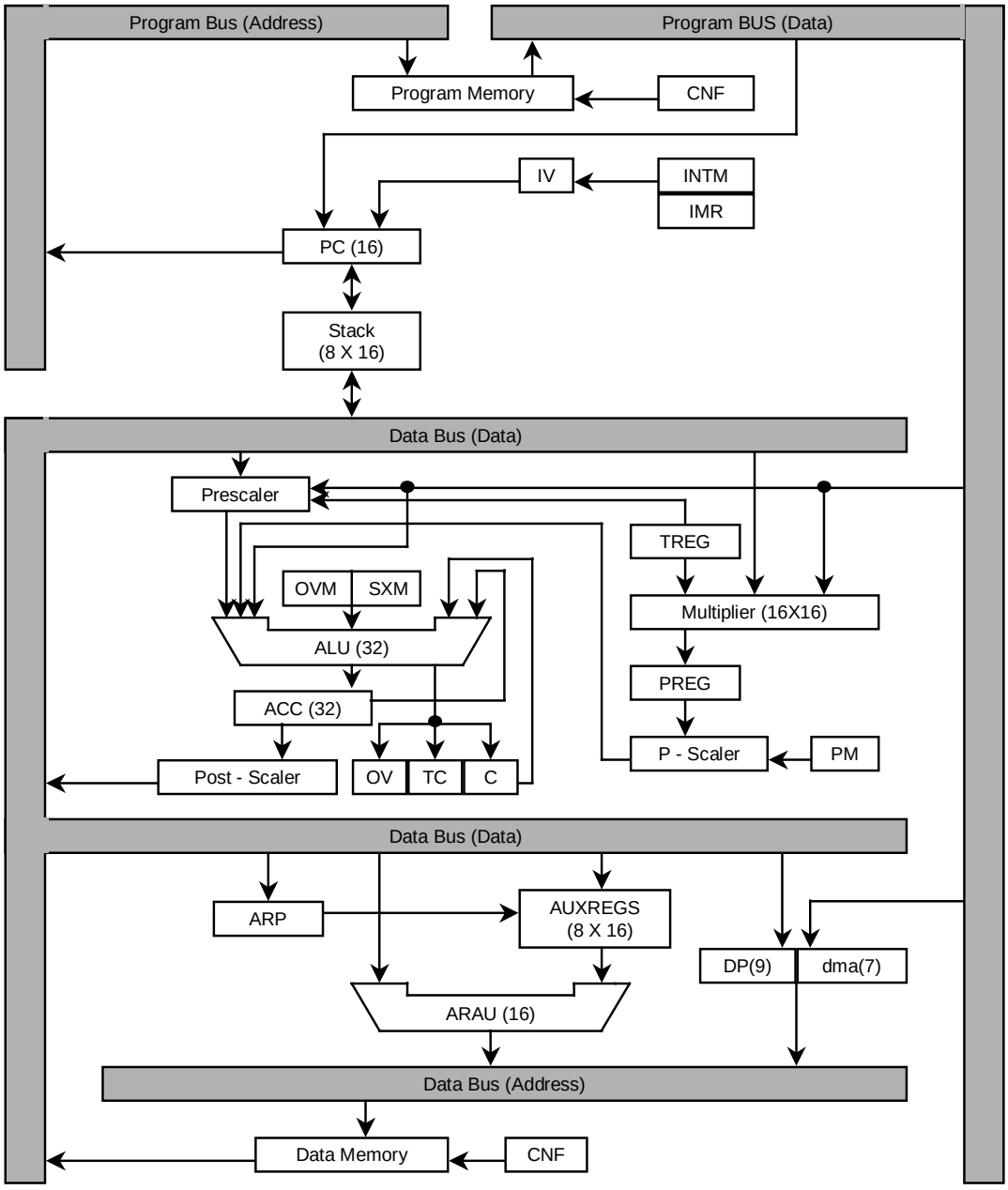
Key Features

- Fast Instruction Cycle Time
- 128K-word total data/program memory space
- On Chip Memory (changeable)
  - 2K 16 bit ROM for program
  - 2K 16 bit single access RAM for program
  - 5K 16 bit dual access RAM for program / data
  - 64 x16 bit dual access RAM for data
- 32-Bit ALU/Accumulator
- 16 x 16-Bit Multiplier With a 32-Bit Product
- Block Moves for Data/Program Management
- Repeat Instructions for Efficient Use of Program Space
- Up to 8 auxiliary registers with dedicated arithmetic unit
- Concurrent DMA using an extended hold operation
- 3 external interrupts, 3 internal interrupts and 1 software interrupt
- Serial Port for Direct CODEC Interface
- Synchronization Input for Synchronous Multiprocessor Configurations
- Wait States for Communication to Slow Off-Chip Memories/Peripherals
- On-Chip Timer for Control Operations
- Instructions for adaptive filtering, FFT, and extended-precision arithmetic
- Bit-reversed indexed-addressing mode for radix-2 FFT
- Built-In on-chip Self Test programs
- Fully Synchronous and Static Design with 35k Core gates
- Supports Test Bench and Full Simulation and Synthesis Scripts

Applications

- Multi-standard Audio Codec (MP3, WMA, AC3 etc.)
- VoIP Voice processor (G.729, G.723.1 etc.)
- Modem data pump (ITU-T V.34, G.DMT, G.VDSL)
- Speech recognition and synthesis
- Echo cancellation

Block Diagram



Internal Blocks

The DSP2 utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of instruction fetch and execution. The DSP2's modification of the Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

Increased throughput on the DSP2 for many DSP applications is accomplished by means of single-cycle multiply/accumulate instructions with a data move option, up to eight auxiliary registers with a dedicated arithmetic unit, and faster I/O necessary for data-intensive signal processing.

(1) Multiplier Multiplies two signed/unsigned 2's complement 16-bit words together and forms signed/unsigned 32-bit result in a single cycle. The product P may be arithmetic shifted left by 0, 1, 4 or right by 6 after execution cycle.

(2) ALU

General-purpose 32 bit 2's complement arithmetic unit

ALU operation:

- Addition
- Absolute value of B
- AND
- Negation
- Complement of B
- OR
- Logical left shift
- Logical right shift
- Subtract
- XOR
- Single bit testing (0 to 15) of A

(3) Program Counter

Provides the present address to the program ROM.

Provides the next address to the pre-fetch address.

Provides the Hardware stack of eight locations.

(4) Addressing Unit

Aux register (AR0-AR7) is selected for loading by the address pointer (ARP) or an immediate pointer contained in the instruction (bits 10-8). AR0 is designated as the index register. It can be used to increment or decrement any other registers. One of the 8 registers is selected by the address pointer in the state register to be an indirect address register for the data RAM.

(5) Decoder

Holds the pre-fetch instruction word from ROM for decoding and data address selection.

- Containing status registers.
- Repeat counter is included.

(6) MMU (Internal and External Memory Management Unit)

Memory management unit is for interfacing between core and memory.

With making only one RAM active, MMU decreases the power consumption.

MMU can make the Block move instruction.

(7) FSM

Controls the sequence of execution of the current instruction.

(8) PLA

The current instruction is taken from either the instruction buffer or from the instruction delay buffer. Provides a control of the current instruction word and state of the micro controller. In addition, the PLA also provides instruction type to FSM, enabling FSM to choose the next microstate properly.

Pin Description

Pin Name	Type	Description
A15 - A0	**Address Bus (O/Z)**	Parallel address bus A15 (MSB) through A0 (LSB). Multiplexed to address external data / program memory or I/O.
D15 - D0	**Data Bus (I/O/Z)**	Parallel data bus D15 (MSB) through D0 (LSB). Multiplexed to transfer data between the DSP2 and external data/program memory or I/O devices.
DS_n **PS_n** **IS_n**	**Data, Program, I/O Selection (O/Z)**	Data, program, and I/O space select signals. Active low.
RW_n	**Read/Write (O/Z)**	Read/write signal. Normally in read mode (high).
STRB_n	**Strobe (O/Z)**	Strobe signal Active low.
RS_n	**Reset (I)**	Reset input
INT0_n **INT1_n** **INT2_n**	**Interrupt Input (I)**	External user interrupts. Prioritized and maskable by the INTM and the IMR.
MPMC_n	**MP/MC (I)**	Microprocessor (high) / microcomputer (low) mode select.
IACK_n	**Interrupt Ack (O)**	Interrupt acknowledge signal.
READY	**Ready (I)**	Data ready input. Indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY=0), waits one cycle and checks READY again.
BR_n	**Bus Request (O)**	Bus request signal. Asserted when the DSP2 requires access to an external global memory
XF	**External Flag (O)**	External flag. Used for signaling other processors in multiprocessor configuration or as a general-purpose output pin.
HOLD_n	**Hold (I)**	Hold input.
HOLDA_n	**Hold Ack (O)**	Hold acknowledge signal.
BIO_n	**Branch Control (I)**	Branch control input. Polled by BIOZ.
CLKOUT	**Clock out (O)**	Clock out signal.
X1	**Output pad for x-tal (O)**	Output pin from the internal oscillator for the crystal. If a crystal is not used, this pin should be left unconnected.
X2/CLKIN	**Input pad for x-tal (I)**	Input pin to the internal oscillator from the crystal, If a crystal is not used, a clock may be input to the device on this pin.

CLKR	**Receive clock input (I)**	Receive clock input. External clock signal for clocking data from the DR pin into the RSR (serial port receive shift register). Must be present during serial port transfers.
CLKX	**Transmit clock input (I)**	Transmit clock input. External clock signal for clocking data from the XSR (serial port transmit shift register) to the DX pin. Must be present during serial port transfers.
DR	**Serial Data Input (I)**	Serial data receive input. Serial data is received in the RSR via this pin.
DX	**Serial Data Output (O/Z)**	Serial data transmit output. Serial data is transmitted from the XSR via this pin. Placed in high -impedance state when not transmitting.
FSR	**Frame Sync for receive input (I)**	Frame synchronization pulses for receive input. The falling edge of the FSR pulse initiates the data-receive process, beginning the clocking of the RSR.
FSX	**Frame Sync for Transmit input/output (I/O/Z)**	Frame synchronization pulses for transmit input/output. The falling edge of the FSX pulse initiates the data-transmit process, beginning the clocking of the XSR. Following reset, the default operating condition of FSX is as an input. This pin may be selected by software to be an output when the TXM bit in the status register is set to 1.

Instructions and Finite State Machine

Type 1 : 1 cycle

ADDK,ADRK,IDLE,LACK,LARK,LDPK,MPYK,RPTK, SBRK,SPM,SUBK,ZAC (12)

Type 2 : 2 cycles

ADLK,ANDK,LALK,LRLK,ORK,RPT,SBLK,XORK (8)

Type 3 : n cycles

ABS,ADD,ADDC,ADDH,ADDS,ADDT,AND,APAC,BIT, BITT,CMPL.CMPR,CONF,DINT,EINT,FORT,LARP,LAC, LACT,LAR,LDP,LPH,LST,LST1,LT,LTA,LTP,LTS,MAR, MPY,MPYA,MPYS,MPYU,NEG,NOP,OR,PAC,POP, POPD,PSHD,RC,RFSM,RHM,ROL,ROR,ROVM,RSXM, RTC,RTXM,RXF,SAR,SC,SFL,SFR,SFSM,SHM,SOVM, SPAC,SQRA,SQRS,SST,SST1,SSXM,STC,STXM,SUB, SUBB,SUBC,SUBH,SUBS,SUBT,SXF,XOR,ZALH,ZALR, ZALS (76)

Type 4 : 1+n cycles

DMOV,IN,LTD,NORM,OUT,PUSH,SACH,SACL,SPH,SPL (10)

Type 6 : 2+n+1 cycles

MAC,MACD,BLKD (3)

Type 7 : 2+n+1 cycles

BLKP,TBLW (2)

Type 8 : 3+n+1 cycles

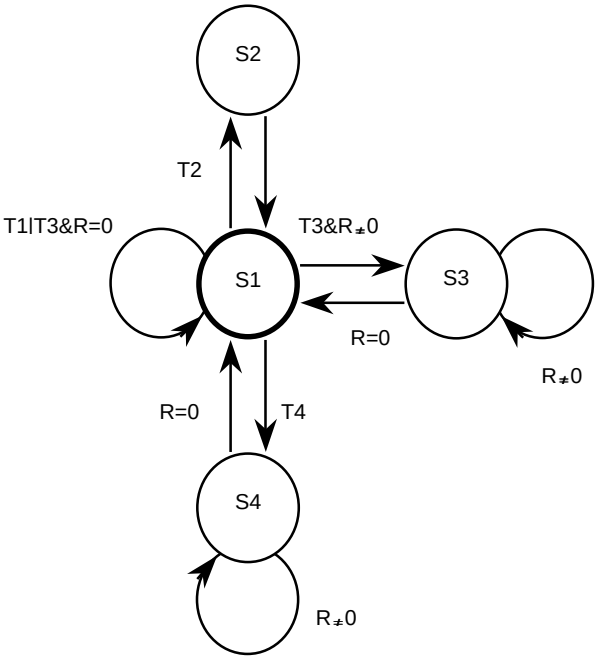
TBLR (1)

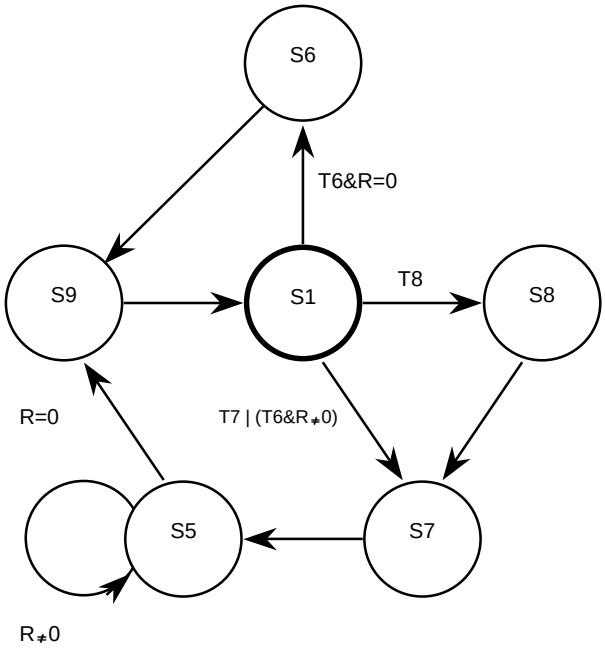
Type 10 : 2/4 cycles

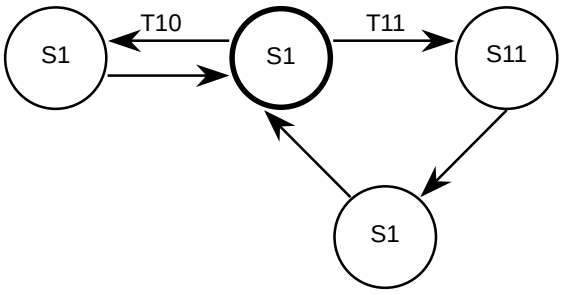
BACC,BANZ,BBNZ,BBZ,BC,BGEZ,BGZ,BIOZ,BLEZ,BLZ, BNC,BNV,BNZ,BV,BZ,CALA (16)

Type 11 : 3 cycles

B,CALL,RET,TRAP, (4)







Verification Methods

- Model Simulation using ASM and C programs
- Gate Level Simulation using ASM and C programs
- FPGA Board Test using Commercial Application Programs
- Silicon Test using Commercial Application Programs

Deliverables

- VHDL Source Code
- Post-Synthesis EDIF Netlist
- Test Bench and Test Vector (VHDL, Verilog)
- Simulation Scripts (Cadence NC-SIM, Verilog-XL)
- Synthesis Scripts (Synopsys Design Compiler)
- Documentation

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